## REMARKS

Claims 1-24 are currently pending in the subject application, and are presently under consideration. Claims 1-9, 11-13 and 15-24 are rejected. Claims 10 and 14 have been indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2, 3 and 11 have been amended. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

### I. Amendments to the Specification

The Related Applications section of the present application has been amended to replace the identified attorney docket numbers with the application serial numbers and to identify the common filing date of the identified applications.

### II. Rejection of Claims 1-6, 9, 11-13, 15-21, and 24 under 35 U.S.C. 102(e)

Claims 1-6, 9, 11-13, 15-21, and 24 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 2005/0251626 to Glasco ("Glasco"). Applicant traverses this rejection for the following reasons.

In contrast to what is recited in claim 1, Glasco fails to teach that a cache state is capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data. In fact, the Office Action relies on sections of Glasco that support the patentability of claim 1. For instance, Par. 45 of Glasco discloses that a memory controller (i.e., is a serialization point) is configured to serialize requests so that only one data access request for a given memory line is allowed at any particular time. Additionally, Par. 87 of Glasco teaches that the memory controller maintains a coherence directory that is accessible by a cache coherency controller. The coherency directory is a mechanism that maintains state information for memory

lines in the system. Glasco at Par. 49 and 87. However, the discussion in Glasco further teaches (consistent with the teachings at Par. 87-90) that the home memory controller is the serialization point for a set of memory lines regardless of the state of such lines. The memory controller employs the state information as well as the occupancy information to reduce the number of transactions that need to be sent to specific clusters. See Glasco at Par. 88-90 and 92 and the table of FIG. 7 for examples of how transactions are serialized at the home memory controller for different cache states and occupancy information. Thus, Glasco teaches that the home memory controller is the serialization point for transactions to memory lines in the coherence directory regardless of the cache state for such memory lines.

Moreover, the reference in the Office Action to Par. 120-123 needs to be considered in its intended context as explained at Par. 124-127 of Glasco. Significantly, Par. 124 states that a sized write request is directed to the home memory controller for the memory line, which serializes the requests for the memory line (after determining that the memory line is a remotely cached dirty memory line) by generating probes to all local nodes. There is no basis from the teachings of Glasco that provides a basis to conclude that claim 1 is anticipated by Glasco. As discussed above, Glasco teaches the home memory controller is the serialization point regardless of the cache state for the memory line. See Table in FIG. 7 and corresponding description at Par. 88-90. Since Glasco fails to disclose claim 1, Applicant respectfully requests reconsideration and allowance of claim 1 and dependent claims 2 to 10.

Claim 2 has been amended to recite that which was believed to be implicit, namely, that the data response includes a copy of the data requested from the second node. Accordingly, no new matter has been added to claim 2. In sharp contrast to claim 2, the cited section of Glasco (Par. 131) does not involve a data response. Instead, Glasco describes a validate block

transaction that is issued to invalidate a memory line to achieve an eviction of the memory line that is not dirty, but clean. Since the process being described is an eviction of clean (as opposed to dirty) memory line, no data response is provided and no data is written back to memory as part of the eviction process. Glasco Par. 128, lines 1 to 4. Moreover, Glasco teaches a transaction called a "validate block" transaction to invalidate the remote copy of the cached data. See Glasco Par. 128, lines 4 to 5, and Glasco Par. 131, lines 1 to 4. The actions being described in Glasco thus differ significantly from what is recited in amended claim 2. For these reasons, Glasco fails to disclose claim 2. Accordingly, applicant respectfully requests reconsideration and allowance of claim 2.

Claim 3 has been amended to recite that which was believed to be implicit, namely, that the ownership data response includes a copy of the data requested from the second node. Accordingly, no new matter has been added to claim 3. Respectfully, the reliance in the Office Action to reject claim 2 (Par. 89-90) to reject claim 3 appears misplaced. Instead, Glasco at Par. 89-90 teaches how a memory controller, operating as a serialization point, utilizes its coherence directory (FIG. 7) when a given memory line is in a modified state and an ownership state, respectively. The context of the Par. 89-90 is for checking an additional field (the dirty data owner information field) for the purpose of reducing the number of transactions in the system. See Glasco, Abstract and at Par. 92. Significantly, none of the description of FIG. 7 (Par. 87-92) teaches or even suggests that a cache state that is capable of identifying a node as an ordering point (from claim 1) that enables such node to provide an ownership data response, as recited in claim 3. Further to the discussion of claim 1, Glasco does not provide an ownership data response that transfers an ordering point to another node, as recited in claim 3. Instead, the home memory controller is the serialization point for a memory line regardless of cache state or a

change in cache state. For these reasons, Glasco fails to disclose claim 3. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 3, as well as dependent claims 4, 5 and 6.

Additionally, claim 4 is patentable over Glasco for at least those reasons presented with respect to claim 2.

The Office Action contends Glasco discloses claim 9. This rejection appears misplaced since claim 9 depends from claim 7, which the Office Action admits is not taught in Glasco. See Office Action at Page 6, lines 10+. How can a dependent claim be anticipated when its base claim or intervening claim is not anticipated? Glasco fails to disclose claim 9 at least for this reason and the reasons stated in support of claim 1, 5, and 7. Applicant respectfully requests reconsideration and allowance of claim 9.

Claim 11 has been amended to recite that the ordering point for the data is identified by a cache state that is associated with the at least one associated cache of one of the processor nodes. Claim 11 thus is patentable over Glasco for substantially similar reasons to those discussed above with respect to claim 1. For example, Glasco fails to teach or even suggest that an ordering point for data can be identified by a cache state, but instead the memory controller in a home cluster operates as a serialization point for a set of memory lines independently of cache state. See Glasco at Par. 112-113. For these reasons and the reasons discussed with respect to claim 1, Glasco fails to disclose the elements of amended claim 11. Accordingly, the Applicant respectfully requests reconsideration and allowance of amended claim 11 and dependant claims 12 to 13.

Regarding claim 15, Glasco fails to teach means for employing a cached ordering point to serialize requests for a block of data from nodes of the system. Similar to as discussed with

respect to claim 1 above, Glasco fails to disclose the use of any cached ordering point as Glasco instead teaches a system in which the home memory controller operates as the serialization point for locally stored memory lines. As a consequence of failing to teach or even suggest a cached ordering point, there is no reason or mechanism disclosed in Glasco to associate such cached ordering for a block of data with a node. Accordingly, the Applicant requests reconsideration and allowance of claim 15, as well as claims 16 to 18 that depend from claim 15. Claims 17 and 18 further are patentable over Glasco for the additional reasons presented with respect to claims 2 and 3, respectively.

Glasco does not anticipate claim 19 for similar reasons as discussed above with respect to claim 1. Significantly, as discussed herein, Glasco does not teach any cache state that identifies a node as being an ordering point for a block of data, as recited in claim 19. Accordingly, the Applicant requests reconsideration and allowance of claim 19.

In addition to their dependence upon allowable claim 19, Glasco fails disclose claims 20 and 21 for the reasons presented above in support of claims 2 and 3. Accordingly, the Applicant requests reconsideration and allowance of claims 20 and 21.

For reasons similar to those discussed above with respect to claim 1, Glasco fails to teach that a cache state might be assigned that defines a node as an ordering point, as recited in claim 24. Instead, Glasco teaches that a memory controller operates as a serialization point without disclosing any relationship between a cache state and an ordering point. Glasco, Par. 45-46. In fact, the various examples of transactions presented in Glasco (see, *e.g.*, Glasco at Par. 80-90) demonstrate that the serialization point is independent of cache state. For example, FIG. 7 shows a coherence directory for a plurality of memory lines having various different states, such as would be implemented in a memory controller acting as the serialization point for the listed

memory lines, regardless of cache state. See Glasco at Par. 87-90. Additionally, Glasco fails to disclose that the coherency protocol is operative to assign a cache state to a cache line, identifying the one node as an ordering point in the system for data. For these reasons and for the reasons discussed with respect to claim 1, Applicant requests reconsideration and allowance of claim 24.

III. **Rejection of Claims 7, 8 and 22-23 under 35 U.S.C. 103(a)**

Claims 7, 8 and 22-23 have been rejected under 35 U.S.C. 103 as being unpatentable over Glasco in view of U.S. Patent Publication number 6,138,218 to Arimilli ("Arimilli"). Applicant traverses this rejection for the following reasons.

For the reasons stated in support of claims 1, 3, and 5, Glasco fails to disclose dependent claim 7. Additionally, Arimilli fails to cure the deficiencies of Glasco since Arimilli fails to teach or suggest what is recited in claim 7. In contrast to the suggestion in the Office Action, the approach disclosed in Arimilli is not that a given node retries its own source broadcast request employing a forward progress protocol, as recited in claim 7. In contrast, Arimilli teaches that the responding cache 114 takes action, such as altering the coherency state associated with requested cache item 208 in its own memory or initiating a push operation to write (modified) requested cache item 208 to system memory. See Arimilli at Col. 5, lines 32-51, and Abstract. That is, the cache 116 that issues the retry 206 does not retry its transaction using any forward progress protocol, but instead it is the responding cache 114 that performs the action to enable an intervention response to proceed. See Arimilli at Col. 5, lines 32-51. For these reasons, Applicant respectfully requests reconsideration and allowance of claim 7.

In addition to the reasons stated in support of claim 7, Glasco in view of Arimilli fails to teach or suggest claim 8. For example, Arimilli fails to teach or suggest any action taken to

achieve forward progress corresponds to a null directory protocol. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 8.

Dependent claim 22 is patentable over Glasco in view of Arimilli at least for the reasons given in support of claim 19 and for the additional reasons presented with respect to claim 7. Accordingly, Applicant respectfully requests withdraw of the rejection of claim 22, as well as claim 22 depending from claim 23.

For at least the reasons given in support of claims 8, 19, 22, dependent claim 23 is patentable over Glasco in view of Arimilli. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 23.

## IV. Allowable Subject Matter

Claims 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant appreciates the allowance of these claims. However, as claims 1 and 10 are allowable over the Glasco, and Glasco in view of Arimilli, it is not necessary to rewrite claims 10 and 14 in independent form. Accordingly, Applicant respectfully requests that the objections to claims 10 and 14 be withdrawn.

## V. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

By: _____

Gary J. Pitzer
Registration No. 39,334
Attorney for Applicant(s)

CUSTOMER NO.: 022879
Hewlett-Packard Company
Legal Department MS 79
3404 E. Harmony Road
Ft. Collins, CO 80528